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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/684,278	10/11/2003	Raymond G. Beausoleil	200311663-1	3329

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EXAMINER	
CONNELLY CUSHWA, MICHELLE R	
ART UNIT	PAPER NUMBER
2874	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/25/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

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Office Action Summary	Application No.	Applicant(s)	
	10/684,278	BEAUSOLEIL ET AL.	
	Examiner	Art Unit	
	Michelle R. Connelly-Cushwa	2874	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 February 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6,17-19,40-42,44-46,48,49,51-58 and 60-62* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *3,4,17-19,40-42,44-46,48 and 49* is/are allowed.

6)☒ Claim(s) *1,2,6,51-58 and 60-62* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 October 2003 and 14 September 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on February 12, 2007 has been entered.

Response to Amendment

Applicant's Amendment filed February 12, 2007 has been fully considered and entered.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 6 and 60-62 are rejected under 35 U.S.C. 103(a) as being unpatentable over Welch et al. (US 7,155,078) in view of Welch et al. (US 2005/0025409 A1).

Regarding claim 1; Figure 64 of Welch et al. ('078) discloses an interconnect system comprising:

- a first circuit unit (TxPIC) integrated on a first chip containing a first electronic circuit and a plurality of modulators (306), wherein:
    - each modulator modulates a corresponding component of a first optical signal output from the first circuit unit;
- a second circuit unit (RxPIC) integrated on a second chip containing a second electronic circuit and a plurality of detectors (290), wherein:
    - the second electronic circuit process a plurality of electrical input signals; and
    - each detector is capable of detecting modulation of a corresponding one of the components of the first optical signal to extract a corresponding one of the input signals.

Welch et al. ('078) does not explicitly state that the first electronic circuit produces a plurality of electrical output signals that control a corresponding one of the modulators. However, in the related patent application publication to Welch et al. (US 2005/0025409 A1), Welch clearly shows that the first electronic circuit of a TxPIC may produce a plurality of electrical output signals that control a corresponding one of the plurality of modulators (see Figures 4, 10 and 11), where each modulator (14 or 106) includes a driver (98, 106A) and bias.

One of ordinary skill in the art would have been motivation to use the TxPIC of the '409 patent application in the system of the '078 patent since both inventions are from the same inventor, are related and the '409 application

provides additional details for the formation and operation of the TxPIC chip, in order to form and use the chip in a manner taught by the inventor of the patent.

Regarding claim 2; Welch et al. does not explicitly teach that the second circuit unit comprises a second plurality of modulators that each modulate a corresponding component of a second optical signal or that the first circuit unit comprises a second plurality of detectors that each detect modulation of one of the components of the second optical signal to extract a corresponding electrical signal. However, optical transceivers are commonly formed in the art by forming both a transmitter and a receiver on the same device in order to enable bi-directional communication. One of ordinary skill in the art would have found it obvious to form a transceiver by including both a transmitter (TxPIC) and a receiver (RxPIC) as disclosed by Welch et al. on each chip, and therefore, would have found it obvious to incorporate a second plurality of modulators that each modulate a corresponding component of a second optical signal in the second circuit unit, and to incorporate a second plurality of detectors that each detect modulation of one of the components of the second optical signal to extract a corresponding electrical signal in the first circuit unit, in order to enable bi-directional communication in the system, since it has been held that a mere reversal of the essential working parts of a device involves only routine skill in the art (*In re Einstein*, 8 USPQ 167) and that mere duplication of the essential working parts of a device involves only routine skill in the art (*St. Regis Paper Co. v. Bemis Co.*, 193 USPQ 8).

Regarding claim 6; Welch et al. teaches that the first light source (lasers, 304) are internal to the first chip and provide the first optical signal to the first circuit unit (TxPIC). However, one of ordinary skill in the art would have found it obvious to provide the first light source external to the first chip in order to allow the chip to be easily incorporated in systems already having the desired light source in place, since it has been held that constructing a formerly integral structure in various elements involves only routine skill in the art (*Nerwin V. Erlichman*, 168 USPQ 177, 179).

Regarding claim 60; Welch et al. does not explicitly state that the first and second chips are mounted on a substrate. However, one of ordinary skill in the art would have found it obvious to mount both the first and second chips on the same substrate in order to allow alignment to be easily maintained once it is achieved and to minimize loss between the two chips during transmission between the two chips by fixing the chips relative to one another.

Regarding claim 61; the source disclosed by Welch includes lasers (304) mounted on a substrate (the chip).

Regarding claim 62; the first and second circuit may be integrated on a single chip as shown in Figure 10 of Welch et al. application '409.

Claims 51-57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Noda et al. (US 2002/0009277 A1).

Regarding claim 51-56; Noda et al. discloses an interface of an integrated circuit (see Figure 2), comprising:

- a waveguide (line defect, 12, forms a waveguide) for an optical signal (23) that includes a plurality of frequency components ($\lambda 1$, $\lambda 2$,... λi, λj);
- a plurality of resonators (point defects, 21 and 22) adjacent to the waveguide (line defect, 12), wherein the resonators respectively correspond to frequency components, and each of the resonators provides a path for a corresponding frequency component; and
- a plurality of electrical elements (photodiodes, 45, 46 and 47; see Figure 8) respectively associated with the resonators;
- wherein the electrical elements (photodiodes) implement transformations between the plurality of frequency components and a plurality of electrical signals;
- wherein the interface comprises a photonic bandgap crystal.

Noda et al. does not explicitly state that the interface is of an electronic integrated circuit or that the electrical signals are processed in an electronic integrated circuit. However, the photodiodes do convert the optical signals into electrical signals, and it is well known in the art that electronic circuits are required to process electronic signals. Therefore, one of ordinary skill in the art would have found it obvious to use the interface disclosed by Noda as an interface of an electronic integrated circuit by connecting the outputs of the photodiodes to an electronic integrated circuit to process the electrical signal

output of the photodiodes to obtain the desired information from the signals or to use the output electrical signals for a desired utility.

One of ordinary skill in the art would have additionally found it obvious to provide a circuit capable of processing a plurality of electrical signals, as discussed above, to use the signals for a desired utility, by integrating both the photodiodes and electrical processing circuit on the same chip to produce a compact device that receives and processes the signals for further use, as the practice of integrating various optical and electrical components on one chip to for optical-electrical circuits to reduce space is established in the art.

Regarding claim 57; Noda et al. further discloses that each of the resonators (point defects) may optionally feed the corresponding frequency components into the waveguide (see paragraph [0059]) in order to form a multiplexer.

Claim 58 is rejected under 35 U.S.C. 103(a) as being unpatentable over Noda et al. in view of Pearsall (US 2004/0150873 A1).

Regarding claim 58; Noda et al. discloses all of the limitations of claim 58 as applied above, except for each of the electronic elements comprising a modulator that modulates the frequency components that the associated resonator feeds into the waveguide and that is controlled by a corresponding one of the electrical signals. Pearsall teaches that electronic elements can be provided adjacent to point defects in photonic crystals to modulate the frequency response of the point defect. One of ordinary skill in the art would have found it obvious to provided electronic elements adjacent to the point defects in the

invention of Noda et al. to modulate the frequency response of the point defects to thereby fine-tune the multiplexed and/or demultiplexed wavelengths as desired. Additionally, one of ordinary skill in the art would have found it obvious to set up a feedback look to control the modulation of the signals to obtain the desired results and therefore, would have found it obvious to control the modulators with a corresponding one of the electrical signals.

Allowable Subject Matter

Claims 3, 4, 17-19, 40-42, 44-46, 48 and 49 are allowed.

The following is a statement of reasons for the indication of allowable subject matter: Claims 3, 4, 17, 44, 46, 48 and 49 remain allowable over the prior art of record for the reason discussed in the prior Office action. Claims 41, 42, 44 and 45 depend from claim 3 and claims 18, 19 and 40 depend from claim 17.

Response to Arguments

Applicant's arguments with respect to claims 1, 2, 6 and 60-62 have been considered but are moot in view of the new ground(s) of rejection.

Regarding the rejections to claims 51-58; Applicant states that Noda fails to disclose or suggest including such a structure in an integrated circuit containing a circuit capable of processing the electronic signal. The integration of additional elements to process the resulting electronic signals is within the level of ordinary skill in the art, as discussed above. Although Noda is primarily concerned with the optical structures, Noda does suggest that the optical signals are converted to electrical signals, and one of ordinary skill in the art would have

recognized that electrical processing circuits to condition the electrical signals as desired for use could be integrated in the invention of Noda et al. to provide a compact structure.

Conclusion

Any inquiry concerning the merits of this communication should be directed to Examiner Michelle R. Connelly-Cushwa at telephone number (571) 272-2345. The examiner can normally be reached 9:00 AM to 7:00 PM, Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rodney B. Bovernick can be reached on (571) 272-2344. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general or clerical nature should be directed to the Technology Center 2800 receptionist at telephone number (571) 272-1562.

MRConnelly-Cushwa

Michelle R. Connelly-Cushwa
Patent Examiner
April 16, 2007